SPECIFICATION

Electronic Version 1.2.8
Stylesheet Version 1.0

OPTOELECTRONIC PACKAGE AND FABRICATION METHOD

Cross Reference to Related Applications

This application is related to commonly assigned US Patent Application No. 10/064581, filed 29 July 2002, entitled "Method and Apparatus for Fabricating Waveguides and Waveguides Fabricated Therefrom," which is herein incorporated by reference.

Background of Invention

[0001] Traditional optoelectronic modules include a large number of discrete components such as laser diodes, fibers, lenses, couplers, electronic driver chips, and signal amplifiers, for example. Each of the different components has different packaging requirements, and efficiently incorporating these different components together in a single module has been a challenge. In single mode waveguide embodiments, for example, optical component attachment typically involves accurate submicron placement (alignment on the order of about 0.25 micrometers) and quick cure adhesives. Conventional methods have included active part alignment with little or no automation which results in high labor costs. Modules are often assembled with a hierarchy of solder materials at different temperatures and wire bonding in very difficult tight spaces. The industry is in need of a low cost automated batch assembly process.

[0002] It would therefore be desirable to provide a hybrid integration packaging process which reduces the manual handling of components and provides passive waveguide alignment and which is useful regardless of whether the mode is single mode or multimode. It would additionally be desirable to provide a packaging process which results in a smaller, lighter module with improved high frequency properties.

Summary of Invention

[0003] Briefly, in accordance with one embodiment of the present invention, a method of fabricating an optoelectronic package comprises: positioning an optical device within a window of a substrate active-side up and below a top substrate surface; filling the window with an optical polymer material; planarizing surfaces of the optical polymer material and the substrate; patterning waveguide material over the optical polymer material and the substrate to form an optical interconnection path and to form a mirror to reflect light from the optical device to the interconnection path; and forming a via to expose a bond pad of the optical device.

[0004] In accordance with another embodiment of the present invention, an optoelectronic package comprises: a substrate; an optical device positioned within a window of the substrate active-side up and below a top substrate surface; an optical polymer material surrounding the optical device within the window and having a planar surface with respect to the top substrate surface; and waveguide material patterned over the optical polymer material and the substrate and forming an optical interconnection path and a mirror configured for reflecting light from the optical device to the interconnection path, the waveguide having a via to expose a bond pad of the optical device.

Brief Description of Drawings

[0005] These and other features, aspects, and advantages of the present invention will become better understood when the following detailed description is read with reference to the accompanying drawings in which like characters represent like parts throughout the drawings, wherein:

[0006] FIGS. 1-10 are sectional side views illustrating stages in fabrication of an optoelectronic package in accordance with one embodiment of the present invention.

[0007] FIGS. 11-17 are sectional side views illustrating stages in fabrication of an optoelectronic package in accordance with another embodiment of the present invention.

[0008] FIGS. 18-20 are sectional side views illustrating stages in fabrication of an optoelectronic package in accordance with another embodiment of the present

invention.

[0009] FIGS. 21-23 are sectional side views illustrating stages in fabrication of an optoelectronic package in accordance with another embodiment of the present invention.

[0010] FIGS. 24-26 are sectional side views illustrating partial views of stages in fabrication of an optoelectronic package in accordance with another embodiment of the present invention.

Detailed Description

[0011] In accordance with one embodiment of the present invention, a method of fabricating an optoelectronic package 1 (FIG. 10), 101 (FIG. 17), 201 (FIG. 23), 301 (FIG. 20) comprises: (a) positioning an optical device 114, 214, 314, 414, 514 (meaning at least one optical device) within a window 12, 112, 212, 312 of a substrate 10 active-side 115 up and below a top substrate surface 11 (FIGS. 1, 12, 18, and 21); (b) filling the window with an optical polymer material 22, 122, 222, 322 (FIGS. 2, 12, 18, and 22); (c) planarizing surfaces of the optical polymer material and the substrate; (d) patterning waveguide material 34, 134, 234, 334 over the optical polymer material and the substrate to form an optical interconnection path 27 (at least one) and to form a mirror 38 (at least one) to reflect light from the optical device to the interconnection path (FIGS. 3-4, 13-14, 18, 22); and (e) forming a via 44 (at least one) to expose a bond pad 116 of the optical device (FIGS. 7, 15, 18, 22).

[0012] As used herein "top," "bottom", and other orientation type words are for purposes of example and not intended to limit or have any relation to the particular orientation of a resulting package in the package's operating environment.

[0013] Substrate 10 typically comprises a thermally conductive material having a low coefficient of thermal expansion (less than or equal to about 3.5, for example) and having good operating properties at high frequencies (in the range of about 10 GHz to about 40 GHz, for example). Example materials include alumina, aluminum nitride, silicon nitride, and carbon fiber filled epoxy resin . It is further advantageous to use a substantially flat substrate 10 (having height variations which do not exceed about 6 micrometers, for example).

[0014] In one embodiment, windows 12 are milled to varying depths which depend upon the thickness of the optical devices 114 and electronic devices 14 (if applicable) to be inserted. In one example, these depths are typically on the order of about 250 micrometers to about 300 micrometers. The thicknesses are typically selected so that the devices can be placed below top substrate surface 11 by at most about 100 micrometers. Although individual windows are shown, multiple devices can be situated in a single window if desired. Additionally, although windows 12 are shown as extending partially through substrate 10, another alternative is to have one or more windows extend completely through the substrate (not shown).

[0015] Typically the positioning of optical device 114 is performed with high precision pick-and-place equipment (not shown). In one embodiment, optical device 114 is attached to substrate 10 with an adhesive 26. Adhesive 26 typically comprises a thermally conductive material and in one embodiment further comprises an electrically conductive material. Solder is particularly useful for conductivity and stability.

[0016] Optical device 114 typically comprises a vertical cavity surface emitting laser (for emitting light 20) or a photodetector. Optical polymer material 22 is selected to have an appropriate optical match with respect to optical device 114. In other words, the optical polymer material does not substantially absorb light at the output wavelength (for emitters) or the detection wavelength (for detectors) of the optical device. In one embodiment the surfaces of optical polymer material 22 and substrate 10 are planarized by polishing.

[0017] Waveguide material 34 typically comprises core and cladding materials as further described below and may be patterned by any desired technique. For single mode applications adaptive patterning such as by a technique described in aforementioned US Patent Application No. 10/064,581 is particularly useful. Mirror 38 is typically formed by creating a desired angle (generally about 45 degrees) of waveguide material 34 over the active portion 18 of optical device 114. Mirror 38 may be fabricated by a conventional stamping or etching technique. If etching is used, one option is a gray scale mask process described in aforementioned US Patent Application No. 10/064,581.

[0018] In a related optoelectronic package 1, 101, 201, 301 embodiment, which may be fabricated in the manner described above with respect to the method embodiment, for example, the package comprises: (a) substrate 10; (b) optical device 114 positioned within window 12 active-side 115 up and below a top substrate surface 11; (c) optical polymer material 22 surrounding the optical device within the window and having a planar surface with respect to the top substrate surface; and (d) waveguide material 34 patterned over the optical polymer material and the substrate and forming an optical interconnection path 27 and a mirror 38 configured for reflecting light from the optical device to the interconnection path, the waveguide having a via 44 to expose a bond pad 116 of the optical device. In this embodiment, "surrounding" means surrounding the exposed sides of optical device 114 except for the locations of one or more vias 44.

[0019] It is typically advantageous to pattern a protective metallization layer 40 over mirror 38 for protecting the surface of mirror 38 from remaining processing steps and the environment. In one embodiment, protective metallization layer 40 comprises aluminum having a thickness ranging from about 1000 angstroms to about 2000 angstroms.

[0020] Additionally, it is typically useful to apply an insulating layer 42 over patterned waveguide material 34. Insulating layer 42, although not required, helps provide dielectric material for improving high frequency properties of the resulting package 1. In such embodiments, via 44 is formed through insulating layer 42 extending to bond pad 116. Typically vias 44 are formed by laser drilling, for example. It is further useful to pattern an electrically conductive interconnection layer 46 extending over insulating layer 42 and into via 44. Electrically conductive interconnection layer 46 may comprise conventional interconnection layers such as titanium, copper, and titanium, for example.

[0021] If desired, one or more additional insulating layers 142 and 242 and electrically conductive interconnection layers 146 and 246 can be added to provide additional flexibility in interconnections (FIG. 9). In another embodiment, interconnections to an electronic device 58 (shown as a high frequency drive electronic module 58 in FIG. 16 which may comprise a module such as described in US Patent No. 5,353,498, for

example) are enhanced by a ball 68 grid array arrangement wherein an electronic die 60 of module 58 is situated in a substrate 70 along with a heat sink 62 and coupled by interconnection layers 64 of module 58 to electrically conductive interconnection layer 346. In this embodiment, floating pad structures 66 such as described in commonly assigned US Patent Nos. 5,900,674 and 6,046,410 can assist in reducing any stress due to coefficient of thermal expansion mismatch. In the ball grid array arrangement, module 58 and the packaged optical device 114 can be tested individually and then assembled to provide higher yield.

[0022] As shown in FIGS. 24-26, in some embodiments where the lower refractive index of air is used to obtain lower loss mirror properties, at least a portion of insulating layer 42 (as well as any overlying insulating layers) extending over the mirror and protective metallization layer 40 is removed (to form an opening 76), and the protective metallization layer is removed from mirror 38. Any insulating layers overlying mirror 38 of material 34 are typically removed by laser ablation, for example. Protective metallization layer 40 is typically removed by standard wet etching techniques, for example. In these embodiments, protective metallization layer 40 acts as a stop for protecting mirror 38 during insulating layer removal. FIGS. 24-26 illustrate close up views of mirror 38 and protective metallization layer 40 before and after material removals. Although the sequence of these material removal acts with respect to the interconnection layer fabrication acts is not critical, it is convenient to perform the material removal prior to the patterning of the outer interconnection layer (layer 246 in FIG. 10 or layer 546 in FIG. 23, for example).

[0023] In one embodiment illustrated in FIG. 2, a lens 24 is positioned over an optical device 214 to focus light 20 onto mirror 38.

[0024] Typically waveguide material 34 comprises a first layer of cladding material 28 over optical polymer material 22 and substrate 10, a layer of core material 30 over first layer of cladding material 28, and a second layer of cladding material 32 over layer of core material 30. In one embodiment, the cladding material comprises benzocyclobutene (BCB) and the core material comprises a polysulfone, for example . In one embodiment, the surface of waveguide material 34 is substantially planar (does not have height variations exceeding about 6.5 micrometers, for example).

[0025] For embodiments wherein optical device 114 has an electrical contact on a surface opposite active side 115, it is useful to provide a substrate 110 comprising a window metallization layer 56 extending at least partially on a bottom surface of the window and top substrate surface 11 (FIG. 11) and to position the optical device so as to at least partially overlie the window metallization layer. In such embodiments, it is particularly useful to use an electrically conductive material as adhesive 126 to attach the optical device and the substrate. In one embodiment, window metallization layer 56 comprises titanium coated by aluminum, for example. In another example embodiment, particularly useful when solder is used as adhesive 126, window metallization layer 56 comprises titanium coated by copper coated by nickel coated by gold.

[0026] In such embodiments, it is additionally useful to have a window 112 comprising a tapered ramp 72 extending between optical device 314 and the portion of top substrate surface 11 underlying window metallization layer 56. The ramp is useful for forming a smooth electrical connection between the portions of the window metallization layer on the window and on the top substrate surface.

[0027] In an even more specific embodiment, substrate 110 comprises a shallow recess 74 in top substrate surface 11 in which window metallization layer 56 is situated. The recess is useful for allowing the metallization to remain after planarizing optical polymer material 22 and substrate 10 surfaces. Although window metallization layer 56 can be patterned prior to surface planarization, patterning is not necessary because planarization can be used to remove metal from the top surface and leave metal in the recesses.

[0028] In addition to or instead of having window metallization layer 56 provide a path for backside die contact, metallization layer 56 may provide a lower metal electrode for a Mach Zender waveguide as can be seen by the example of the portion of metallization layer 56 underlying microstrip reference plane 240 in FIG. 14.

[0029] In a more specific embodiment, which may be separate from or combined with the window metallization layer embodiment, microstrip reference plane 240 is patterned over the waveguide material. Typically deposition and patterning of microstrip reference plane 240 is performed simultaneously with that of protective metallization

layer 140 over mirror 138. In an even more specific embodiment wherein window metallization layer 56 and microstrip reference plane 240 are both present, a plurality of vias 44 are formed with at least one via extending to microstrip reference plane 240 and at least one via extending to a portion of the window metallization layer 56 situated on top substrate surface 11 (FIG. 15). In a still more specific embodiment, the electrical interconnection is provided by an electrically conductive interconnection layer 346, 446 (FIG. 15) overlying the insulating layer. As described in Gregory Phipps, Flip-Chip Packaging moves into the Mainstream, *Semiconductor International*, 1 September 2002, microstrip structures typically include a signal conductor over a parallel reference plane separated by a dielectric material and provide benefits of controlled signal impedance, reduced signal cross talk, and reduced signal inductance.

[0030] In a more specific embodiment, as shown in FIGS. 19-20, which again may be separate from or combined with the window metallization layer embodiment, substrate 310 comprises a first stripline reference plane 41 patterned thereon, and a second stripline reference plane 746 is patterned over at least a portion of electrically conductive interconnection layer 646 (and insulating layer 742). Typically first stripline reference plane 41 is patterned on substrate 310 after the surfaces of substrate 310 and optical polymer material 322 are planarized. In these embodiments, first stripline reference plane 41 is designed to be thin enough (about 2 micrometers to about 4 micrometers in one example) so as not to interfere with the flatness specification (6.4 micrometers in this example). As described in aforementioned Gregory Phipps, Flip-Chip Packaging moves into the Mainstream, stripline structures typically include a signal conductor layer sandwiched between two reference plane layers on the top and bottom with dielectric layer between each combination of signal conductor and reference plane layers and provide benefits of high speed signal transmission, reduced cross talk and noise coupling, and good signal coupling.

[0031] In a related stripline embodiment which may be used in addition or instead of the embodiment with the first stripline reference plane 41 on the substrate, a first stripline reference plane 440 is patterned on the waveguide material.

[0032] In an even more specific embodiment a plurality of vias 44 are formed with at

least one via extending to first stripline metallization layer 41 and at least one via extending to a portion of window metallization layer 56 situated on the top substrate surface.

[0033] In another embodiment, as shown in FIGS. 1-10 for example, the optoelectronic package further includes an electronic device 14 (at least one) positioned within the at least one window 12 of the substrate 10 active-side 15 up, and vias 44 expose bond pads 16 of the electronic device. In this embodiment, the exposed bond pads of the electronic and optical devices are electrically interconnected. In a more specific embodiment, insulating layer 42 is applied over the patterned waveguide material, and an electrically conductive interconnection layer 46 extends over the insulating layer and into the vias to provide the electrical interconnections. In another more specific embodiment, a heat sink 54 is attached to a surface of the substrate opposite the top substrate surface. One non-limiting example of a heat sink is a thermoelectric cooler. Electronic device 14 may comprise either a single chip (FIG. 1) or a multichip module 158 (FIG. 21).

[0034] In another embodiment a portion 48 of the insulating layer is removed to expose the patterned waveguide material and an optical fiber 50 is attached to the exposed patterned waveguide material by an optical connector 52 (FIG. 10). Alignment of the fiber can be accomplished, for example, by using standard active processes or by using passive processes such self-aligned solder connection techniques or MEMS alignment techniques (not shown).

[0035] The above embodiments have been described generally and can be combined in any one of a number of suitable combinations. Several exemplary combinations are described below but are not intended to be limiting.

[0036] FIGS. 1-10 are sectional side views illustrating stages in fabrication of an optoelectronic package in accordance with one embodiment of the present invention wherein an optoelectronic package 1 comprises: (a) a substrate 10 having windows 12; (b) an optical device 114 positioned within a first window 12 of the substrate active-side 115 up and below a top substrate surface 11; (c) an electronic device 14 positioned within a second window of the substrate active-side up 15 and below the top substrate surface; (d) an optical polymer material 22 surrounding the optical

device within the first window and having a planar surface with respect to the top substrate surface; (e) filler material 23 surrounding the electrical device within the second window and having a planar surface with respect to the top substrate surface; (f) waveguide material 34 patterned over the optical polymer material, filler material, and the substrate and forming an optical interconnection path 27 and a mirror 38 configured for reflecting light from the optical device to the interconnection path; (g) an insulating layer 42 over the patterned waveguide material, the insulating layer and waveguide material having vias 44 extending therethrough towards bond pads of the electrical and optical devices; and (h) an electrically conductive interconnection layer 46 extending over the insulating layer and into the vias. As described above, it is generally advantageous to further include a protective metallization layer 40 over the mirror. Alternatively, it is advantageous to include an opening 76 in the insulating layer exposing at least a portion of the mirror.

[0037] Although not required (because optical properties of the material over the electrical device are not important), typically filler material 23 is the same material as optical material 22. Additional useful features which are also described above include window metallization layer 56 and microstrip reference plane 240. Other useful features include heat sink 54 attached to a surface of the substrate opposite the top substrate surface and having the electronic device comprise a multichip module 158.

[0038] FIGS. 11-17 are sectional side views illustrating stages in fabrication of an optoelectronic package in accordance with another embodiment of the present invention wherein an optoelectronic package 101 comprises: (a) a substrate 110 having a window 112 and comprising a window metallization layer 56 extending at least partially on a bottom surface of the window and a top substrate surface 11; (b) an optical device 314 positioned within the window active-side 115 up and below the top substrate surface at least partially overlying the window metallization layer; (c) an optical polymer material 122 surrounding the optical device within the window and having a planar surface with respect to the top substrate surface; (d) waveguide material 134 patterned over the optical polymer material and the substrate and forming an optical interconnection path 27 and a mirror 138 configured for reflecting light from the optical device to the interconnection path; (e) a microstrip reference plane 240 over the waveguide material; (f) an insulating layer 342 over the waveguide

material and microstrip reference plane, the insulating layer and waveguide material having vias 144 extending therethrough towards bond pads of the electrical and optical devices, the window metallization layer, and the microstrip reference plane; and (g) an electrically conductive interconnection layer 346, 446 extending over the insulating layer and into the vias. As described above, it is generally advantageous to further include a protective metallization layer 40 over the mirror. Alternatively, it is advantageous to include an opening 76 in the insulating layer exposing at least a portion of the mirror.

[0039] An additional useful feature which is also described above include a solder 126 configured for coupling the optical device and the substrate. Other example useful features include the electrically conductive interconnection layer 446 coupling the microstrip reference plane and the substrate window metallization layer as well as heat sink 154 and heat sink 62 (FIG. 17).

[0040] FIGS. 18-20 are sectional side views illustrating stages in fabrication of an optoelectronic package in accordance with another embodiment of the present invention wherein an optoelectronic package 301 comprises: (a) a substrate 310 having a window 312 and comprising a window metallization layer 56 extending at least partially on a bottom surface of the window and a top substrate surface 11 and a first stripline reference plane 41 patterned on the substrate; (b) an optical device 114 positioned within the window active-side 115 up and below the top substrate surface at least partially overlying the window metallization layer; (c) an optical polymer material 322 surrounding the optical device within the window and having a planar surface with respect to the top substrate surface; (d) waveguide material 334 patterned over the optical polymer material and the substrate and forming an optical interconnection path 27 and a mirror 338 configured for reflecting light from the optical device to the interconnection path; (e) an insulating layer 542 over the waveguide material, the insulating layer and waveguide material having vias 44 extending therethrough towards bond pads of the electrical and optical devices, the window metallization layer, and the first stripline reference plane; and (f) an electrically conductive interconnection layer 646 extending over the insulating layer and into the vias; and (g) second stripline metallization layer 746 patterned over the electrically conductive interconnection layer.

[0041] As described above, it is generally advantageous to further include a protective metallization layer 340 over the mirror. If a portion of first stripline reference plane 440 is situated over the waveguide material, typically protective metallization layer 340 will be the same material as first stripline reference plane 440. Alternatively, it is advantageous to include an opening 76 in the insulating layer exposing at least a portion of the mirror.

[0042] An additional useful feature which is also described above include a solder 126 configured for coupling the optical device and the substrate. Other example useful features include the substrate window metallization layer as well as heat sink 54 (FIG. 10) and/or heat sink 62 (FIG. 20).

[0043] FIGS. 21-23 are sectional side views illustrating stages in fabrication of an optoelectronic package in accordance with another embodiment of the present invention wherein an optoelectronic package 201 comprises: (a) a substrate 210 having windows, a first window 213 having a window metallization layer 56 extending at least partially on a bottom surface of the first window and a top substrate surface 11; (b) an optical device 414 positioned within the first window active-side 115 up and below the top substrate surface at least partially overlying the window metallization layer; (c) a multichip module 158 positioned within a second window 212 of the substrate active-side up and below the top substrate surface; (d) an optical polymer material 222 surrounding the optical device within the first window and having a planar surface with respect to the top substrate surface; (e) filler material 223 surrounding the electrical device within the second window and having a planar surface with respect to the top substrate surface; (f) waveguide material 234 patterned over the optical polymer material, filler material, and the substrate and forming an optical interconnection path 27 and a mirror 238 configured for reflecting light from the optical device to the interconnection path; (g) a microstrip reference plane 240 over the waveguide material; (h) an insulating layer 242 over the patterned waveguide material and the microstrip reference plane, the insulating layer and waveguide material having vias 44 extending therethrough towards bond pads of the multichip module and the optical device, the window metallization layer, and the microstrip reference plane; and (i) an electrically conductive interconnection layer 546 extending over the insulating layer and into the vias. As described above, it is generally

advantageous to further include a protective metallization layer 140 over the mirror. Alternatively, it is advantageous to include an opening 76 in the insulating layer exposing at least a portion of the mirror.

[0044] Additional useful features which are also described above include heat sink 54 and solder 26 configured for coupling the optical device and the substrate.

[0045] The embodiment of FIGS. 21-23 does not involve ball grid array attachment and results in a smaller more compact integrated module.

[0046] While only certain features of the invention have been illustrated and described herein, many modifications and changes will occur to those skilled in the art. It is, therefore, to be understood that the appended claims are intended to cover all such modifications and changes as fall within the true spirit of the invention.